What is claimed is:

1. A memory device which includes at least one bank having first and second unit blocks, each containing a plurality of cell arrays and first and second decoding units for decoding an inputted column address and outputting column selecting signals of the first and second unit blocks, comprising:

a column address transmitting unit for simultaneously enabling the first and second decoding unit, regardless of a bit select block signal, which selects the first or second unit blocks, of the inputted column address during a test mode;

a first combining circuit for combining test data outputted by the column selecting signal of the first unit blocks and detecting an error of the test data in the test mode;

a second combining circuit for combining test data outputted by the column selecting signal of the second unit blocks and detecting an error of the test data in the test mode; and

a first and a second output pads for individually outputting each of outputted signals from the first and second combining circuits.

2. The memory device as recited in claim 1, wherein the column address transmitting unit selectively enables the first

or the second decoding unit in response to the bit select block signal during a normal mode.

3. The memory device as recited in claim 2, wherein each of the first and second combining circuits includes:

first to forth exclusive NOR gates for receiving data of each group having a same value among the whole test data;

first and second NAND gates for individually receiving each two output signals of the four NOR gates; and

a NOR gate for receiving output signals of the first and second NAND gate.

4. A memory device which includes at least one bank having first and second unit blocks, each having a plurality of cell arrays, a counting unit for counting an inputted column address by a burst length and thereon outputting, and first and second decoding unit for decoding an inputted column address and outputting column selecting signals of the first and second unit blocks, comprising:

a test mode controller for simultaneously enabling the first and second decoding unit, regardless of an outputted column address from the counting unit during a test mode;

a first combining circuit for combining test data outputted by the column selecting signal of the first unit blocks and detecting an error of the test data in the test mode;

a second combining circuit for combining test data

outputted by the column selecting signal of the second unit blocks and detecting an error of the test data in the test mode; and

first and second output pads for individually outputting each of outputted signals from the first and second combining circuits.